	L #	Hits	Search Text	DBs
1	L1	12820	register near10 (size format type length width) near5 (operand data)	USPAT; US-PGPUB
2	L3	2939	(enabl$3 activ$5 us$3 utiliz$3) near99 1	USPAT; US-PGPUB
3	L8	1922611	(enabl$3 activ$5 us$3 utiliz$3) near20 (part$5 portion select$4 correspond$3 respective)	USPAT; US-PGPUB
4	L9	428	8 near99 1	USPAT; US-PGPUB
5	L11	42	9 near99 operand	USPAT; US-PGPUB
6	L12	3551	register near10 (size format type length width) near5 (operand data)	EPO; JPO; DERWENT; IBM_TDB
7	L13	507	(enabl$3 activ$5 us$3 utiliz$3) near99 12	EPO; JPO; DERWENT; IBM_TDB
8	L14	1155057	(enabl$3 activ$5 us$3 utiliz$3) near20 (part$5 portion select$4 correspond$3 respective)	EPO; JPO; DERWENT; IBM_TDB
9	L15	96	14 near99 12	EPO; JPO; DERWENT; IBM_TDB

	Document ID	U	Title	Current OR
1	JP 20030 36247 A	☐	ID AND PASSWORD INPUT SUPPORT SYSTEM	
2	JP 20011 67570 A	☒	LINE MEMORY DEVICE	
3	JP 20000 90105 A	☒	DOCUMENT MANAGING METHOD AND DOCUMENT MANAGEMENT AND RETRIEVAL SYSTEM	
4	JP 20000 22807 A	☒	PHS(R) TELEPHONE SET WITH PERSONAL INFORMATION TRANSMISSION/RECEPTION FUNCTION	
5	JP 11102 207 A	☒	MEMORY RELAY	
6	JP 11053 206 A	☒	PROCESSOR	
7	JP 10134 036 A	☒	SINGLE-INSTRUCTION MULTIPLE DATA PROCESSING FOR MULTIMEDIA SIGNAL PROCESSOR	
8	JP 09246 993 A	☒	RECEPTION DATA PROCESSING CIRCUIT	
9	JP 09180 434 A	☒	DATA PROCESSOR	
10	JP 09139 070 A	☒	SEMICONDUCTOR STORAGE SYSTEM	
11	JP 09058 066 A	☒	PRINTER WITH FUNCTION OF PREVENTING PRINT FLAW	
12	JP 09016 851 A	☒	AUTOMATIC ELECTRONIC INFORMATION VENDING DEVICE AND ELECTRONIC INFORMATION PROCESSOR	
13	JP 08095 999 A	☒	DEVICE AND METHOD FOR RETRIEVING DATA	
14	JP 07244 681 A	☒	CAD SYSTEM UTILIZING FEATURE	
15	JP 07212 413 A	☒	RECEPTION CIRCUIT FOR ASYNCHRONOUS DATA	
16	JP 07199 904 A	☒	AUTOMATIC CORRECTING CIRCUIT FOR HORIZONTAL DISPLAY POSITION	
17	JP 07044 354 A	☒	SIGNAL PROCESSOR	
18	JP 06111 594 A	☒	SEMICONDUCTOR MEMORY DEVICE	
19	JP 06042 978 A	☒	MOTION-DISTANCE MEASURING APPARATUS	
20	JP 05324 539 A	☒	SEMICONDUCTOR DEVICE	
21	JP 05298 078 A	☒	SOFTWARE PARTS MANAGEMENT AND RETRIEVAL DEVICE	

	Document ID	U	Title	Current OR
22	JP 05282 132 A	☒	PEAK/BOTTOM HOLDING CIRCUIT	
23	JP 05265 750 A	☒	ARITHMETIC UNIT	
24	JP 05207 264 A	☒	PICTURE MEMORY DEVICE FOR LONGITUDINAL LATERAL SIZE CONVERSION	
25	JP 05204 635 A	☒	REGISTER CONTROL SYSTEM	
26	JP 05197 734 A	☒	DATA PROCESSING SYSTEM	
27	JP 05134 848 A	☒	DATA SHIFT CIRCUIT FOR CENTRAL PROCESSING UNIT	
28	JP 05002 400 A	☒	SPEECH RECOGNITION DEVICE	
29	JP 04294 456 A	☒	METHOD FOR SYNTHESIZING DATA TRANSFER ROUTE	
30	JP 04081 670 A	☒	PULSE AMPLITUDE DATA SAMPLING CIRCUIT	
31	JP 03137 712 A	☒	INITIAL STATE SETTING CIRCUIT	
32	JP 01233 573 A	☒	PICTURE DATA STORAGE DEVICE	
33	JP 01035 491 A	☒	DRIVING SYSTEM FOR DISPLAY DEVICE	
34	JP 64001 546 A	☒	CONTROL APPARATUS OF OPTICAL WRITING PRINTER	
35	JP 63286 936 A	☒	REGISTER CIRCUIT	
36	JP 63282 531 A	☒	REGISTER CIRCUIT	
37	JP 61279 969 A	☒	DATA BUFFER CONTROL SYSTEM	
38	JP 61255 450 A	☒	SEMICONDUCTOR MEMORY DEVICE	
39	JP 61204 754 A	☒	DATA TRANSFER DEVICE	
40	JP 61204 753 A	☒	DATA TRANSFER DEVICE	
41	JP 60171 547 A	☒	INFORMATION MEMORY	
42	JP 60021 270 A	☒	DATA OUTPUT SYSTEM	
43	JP 59065 361 A	☒	MICROCOMPUTER CIRCUIT DEVICE	
44	JP 58050 039 A	☒	LIST OUTPUT METHOD	

	Document ID	U	Title	Current OR
45	JP 56011 527 A	☒	CLOCK CONTROL SYSTEM	
46	JP 55033 246 A	☒	SELECTIVE CONTROL SYSTEM FOR REGISTER	
47	JP 54148 330 A	☒	BUFFER MEMORY CONTROL SYSTEM	
48	WO 94248 23 A1	☒	ADAPTIVE VIDEO COMPRESSION USING VARIABLE QUANTIZATION	
49	EP 54028 5 A2	☒	Method and apparatus for floating point normalisation.	
50	US 66465 76 B	☒	Data parsing system for telecommunication industry, has operational logic to receive enable signals and selectively connected storage units as inputs and derive array of output data bits related to desired register format	
51	US 20030 13584 4 A	☒	Computer system operation method involves emulating marked successive instructions whose data type snapshot are modified on merging with current data type usage map	
52	US 65713 30 B	☒	Computer processor, has execution core to execute instruction prefix which specifies that established default operand size of specified bits is overridden with different operand size	
53	JP 20031 69186 A	☒	Facsimile for real-time internet facsimile communication, controls device operation so that type of selection information input by user during call or dial data registration, agrees with communication path	
54	JP 20023 19059 A	☒	Automatic cash handling apparatus e.g. ATM in bank, recognizes payment form entry data based on registered transfer place data and corresponding format information, and updates account based on payment information from user	
55	KR 20020 74565 A	☒	Device and method for data filtering, having programmable field	
56	KR 20020 51099 A	☒	Method for storing data in telephone	
57	EP 11848 35 A	☒	Multi-format sampling register for data driver of active matrix display, has digital-to-analog converter which is switched ON and OFF in high resolution and low resolution modes, respectively	
58	US 62925 06 B	☒	Length selectable method of generating spread spectrum communication scrambling pseudorandom signal e.g. for communication systems, where data entry is directed into pseudorandom number generator IC chip controlling registers	
59	US 62791 02 B	☒	Combined rename table employing method for processor and computer, involves writing names of physical register and class of data format required by micro-operation in respective fields	
60	US 60091 39 A	☒	Asynchronous programmable frequency divider circuit e.g. for PLL	
61	JP 10241 049 A	☒	Accounts apparatus e.g. electronic cash register, POS terminal - converts data format to enable processing of visitor purchase goods corresponding to selected application software	
62	US 57404 41 A	☒	Bytecode program interpreter method - involves preprocessing program by determining whether execution of any instruction within program would violate data type restrictions for that instruction	
63	JP 08265 159 A	☒	Binary coded decimal notation conversion circuit for transforming BCD data to binary data - uses single bit adder and zero conversion module to process fine bits or more starting from lower order bits while using constant selector to guide data from holding register to one bit adder	

	Document ID	U	Title	Current OR
64	US 5557666 A	☒	Absence message displaying in private exchange system - enabling party to register absence message indicating reason do absence and its term either in time or data format then detecting whether absence message has been registered when incoming call is received	
65	JP 08106544 A	☒	Image processing method for background drawings in TV game machines - involves forming specific content of image data repeatedly by using plain size register unit which corresponds to map register selector and pattern name controller	
66	JP 07244681 A	☒	Computer aided design system converts portion of design data specified by user, to predetermined format as feature and registers converted data as new feature	
67	JP 07306784 A	☒	Register management appts. limiting increase in command word length - has separate address and data registers, command deciphering part determining register switching flag, with each instruction having limit in type of register that can be used NoAbstract	
68	US 5457694 A	☒	Advanced technology attachment interface signals recording-interpreting appts - has trigger circuit to select starting and stopping point of recording, while event recognition circuit limits recording to certain valid events	
69	US 5909250 A	☒	Compressing video data using compression coding - using control registers holding compression parameters which are automatically updated according to size sensed from compressing data portion	
70	EP 614137 A	☒	Providing extensible register esp. for data processing system - has register containing two register portions which are modified by instructions received	
71	JP 06203107 A	☒	Layout editor device for layout pattern of e.g. semiconductor integrated circuit using CAD - registers size and coordinate data of cell, creates layout pattern and selects cell for registration into cell, and specifies direction and distance of movement for each group of cells NoAbstract	
72	JP 06105285 A	☒	Variable-length coded data reproducer - zeroes register output signal and AC components from controller using selector control signal to decode DC components only for reproduction NoAbstract	
73	JP 06021782 A	☒	Pseudo random signal generating circuit - adds data selector to D-type flip=flop each forming shift register to eliminate adjustment of phase difference between clock and enable signals NoAbstract	
74	EP 574900 A	☒	Transferring data in computer between client and server application - has multiple data formats stored in persistent registry for user to select and client application requesting data from server in selected format	
75	EP 207519 B	☒	Interpreting and executing tagged and un-tagged instructions - reads and executes instruction from memory, decodes instruction which are either pure data type or have tag and data parts	
76	US 5175819 A	☒	FIFO buffer with expandable parallel to serial conversion - has tap-shift register which controls conversion, receives serial-input-expansion input signal and develops serial-output-expansion output signal	
77	EP 415461 A	☒	Central processing unit supporting variable length instructions - selects number of data path elements based on either size code or size field, selection depending on size field	
78	EP 390309 A	☒	Parallel data word unpacking apparatus - receives parallel packed input data words with fixed width of bits and outputs words with variable width	
79	EP 376905 A	☒	Programmable integrated logic device - has programmable logic arrays arranged in mosaic layout together with intermingled arranged interfacing blocks	
80	EP 301636 A	☒	Transceiver arrangement for full-duplex data transmission - has echo canceller and hybrid junction connecting transmitter receiver and two-wire parts	
81	DD 259985 A	☒	Recording circuit for processing states of CPU - has number of registers that are selected for buffering and subsequent storing in memory of various lengths of data	

	Document ID	U	Title	Current OR
82	EP 248297 B	☒	Chip selection and counting in DPWM IC - latching PWM bits into PWM latch and shift register if eight bit update is received by DPWM from user microcomputer	
83	US 4744043 A	☒	Data processor execution unit providing multiple aritmetric formats - uses operand of instruction to select number of registers containing operands for use by arithmetic unit	
84	EP 317567 B	☒	Peripheral control circuitry for personal computers - uses custom NMOS 48 pin chip interfacing with data bus and address bus architecture of host processor using DMA	
85	EP 248297 B	☒	Microprocessor interface controlled - has clock divider connected in DPWM to generate and present clock signals throughout DPWM	
86	US 4649477 A	☒	Data processor with operand size mechanism - has instruction register selectively enabled by size control selector with bus and multiplexer routing instructions	
87	EP 207519 A	☒	Data processor executing two data types - has decoders to distinguish if tags are present and what format of tag is used for address compilation	
88	EP 155211 A	☒	By=pass control system in pipeline control of computer - reduces delay in operation due to register conflict during flow of pipeline operation	
89	FR 2552903 A	☒	Hardware multiplier using pipeline processing of data packets - delivers result in same format and uses approximation register for multiplier and selector to extract multiplier component	
90	EP 110642 A	☒	Microcomputer with multiple-register processor - has addressable memory locations and uses instructions having same bit size and format, with reduced decoding delays	
91	SU 890400 B	☒	Central processing unit - has extra mode unit and instruction decoder, with inputs from storage unit, and mode unit outputs to register	
92	EP 319507 A	☒	Serial-access memory device with variable shift length stored data - uses matrix of memory cells selected by shift registers with externally-applied shift length designation signal	
93	SU 798797 B	☒	Binary to redundant cyclic code converter - uses controller signal to initiate interrogation of most significant digit lines through register	
94	US 4190835 A	☒	Editing display system with dual cursors - uses set of memories connected to processor with several control circuits connected to display unit, keyboard and other input-output systems	
95	SU 638993 A	☒	CRT display for automatics and computing - uses line selector connected to control unit, symbol code register and line former to display variable size alphanumerical and symbol data	
96	US 4079372 A	☐	Serial to parallel data converter - uses control data in incoming pulse train to regulate operation of converter	

	Document ID	U	Title	Current OR
1	US 20030 22108 9 A1	☐	Microprocessor data manipulation matrix module	712/221
2	US 20030 20851 8 A1	☒	Generic implementations of ellipitic curve cryptography using partial reduction	708/492
3	US 20030 17224 9 A1	☒	Methods of performing DSP operations with complex data type operands	712/35
4	US 20030 16745 8 A1	☒	Programmatic access to the widest mode floating-point arithmetic supported by a processor	717/114
5	US 20030 15436 0 A1	☒	Methods of performing DSP operations using flexible data type operands	712/210
6	US 20030 13584 4 A1	☒	Bytecode program interpreter apparatus and method with pre-verification of data type restrictions and object initialization	717/126
7	US 20030 07921 0 A1	☒	Integrated register allocator in a compiler	717/152
8	US 20030 05613 4 A1	☒	Method and apparatus for power reduction in a digital signal processor integrated circuit	713/324
9	US 65606 94 B1	☒	Double prefix overrides to provide 16-bit operand size in a 32/64 operating mode	712/210
10	US 65570 96 B1	☒	Processors with data typer and aligner selectively coupling data bits of data buses to adder and multiplier functional blocks to execute instructions with flexible data types	712/221
11	US 64703 76 B1	☒	Processor capable of efficiently executing many asynchronous event tasks	718/108
12	US 63341 36 B1	☒	Dynamic 3-level partial result merge adder	708/710
13	US 62984 38 B1	☒	System and method for conditional moving an operand from a source register to destination register	712/226
14	US 62567 82 B1	☒	Compile apparatus, compile method and computer-readable medium storing compiler	717/151
15	US 62471 71 B1	☒	Bytecode program interpreter apparatus and method with pre-verification of a data type restrictions and object initialization	717/126
16	US 61733 66 B1	☒	Load and store instructions which perform unpacking and packing of data bits in separate vector and integer cache storage	711/129
17	US 61548 31 A	☒	Decoding operands for multimedia applications instruction coded with less number of bits than combination of register slots and selectable specific values	712/208
18	US 61416 73 A	☒	Microprocessor modified to perform inverse discrete cosine transform operations on a one-dimensional matrix of numbers within a minimal number of instructions	708/402
19	US 60866 32 A	☒	Register optimizing compiler using commutative operations	717/146
20	US 60615 21 A	☒	Computer having multimedia operations executable as two distinct sets of operations within a single instruction cycle	712/9

	Document ID	U	Title	Current OR
21	US 6047372 A	☒	Apparatus for routing one operand to an arithmetic logic unit from a fixed register slot and another operand from any register slot	712/222
22	US 6009505 A	☒	System and method for routing one operand to arithmetic logic units from fixed register slots and another operand from any register slot	712/6
23	US 5999731 A	☒	Bytecode program interpreter apparatus and method with pre-verification of data type restrictions and object initialization	717/126
24	US 5941938 A	☒	System and method for performing an accumulate operation on one or more operands within a partitioned register	708/490
25	US 5909572 A	☒	System and method for conditionally moving an operand from a source register to a destination register	712/226
26	US 5893145 A	☒	System and method for routing operands within partitions of a source register to partitions within a destination register	711/125
27	US 5881259 A	☒	Input operand size and hi/low word selection control in data processing systems	712/210
28	US 5832533 A	☒	Method and system for addressing registers in a data processing unit in an indexed addressing mode	711/2
29	US 5801975 A	☒	Computer modified to perform inverse discrete cosine transform operations on a one-dimensional matrix of numbers within a minimal number of instruction cycles	708/402
30	US 5740441 A	☒	Bytecode program interpreter apparatus and method with pre-verification of data type restrictions and object initialization	717/134
31	US 5440749 A	☒	High performance, low cost microprocessor architecture	712/206
32	US 5394558 A	☒	Data processor having an execution unit controlled by an instruction decoder and a microprogram ROM	712/211
33	US 5099445 A	☒	Variable length shifter for performing multiple shift and select functions	708/209
34	US 4827402 A	☒	Branch advanced control apparatus for advanced control of a branch instruction in a data processing system	712/234
35	US 4785411 A	☒	Cascade filter structure with time overlapped partial addition operations and programmable tap length	708/322
36	US 4649477 A	☒	Operand size mechanism for control simplification	712/210
37	US 4355555 A	☒	Address generating mechanism for multiple virtual spaces	711/208
38	US 4258419 A	☒	Data processing apparatus providing variable operand width operation	712/210
39	US 4250545 A	☒	Data processing apparatus providing autoloading of memory pointer registers	712/208
40	US 4240142 A	☒	Data processing apparatus providing autoincrementing of memory pointer registers	712/42
41	US 4176394 A	☒	Apparatus for maintaining a history of the most recently executed instructions in a digital computer	712/227
42	US 4037213 A	☐	Data processor using a four section instruction format for control of multi-operation functions by a single instruction	712/212